ABSTRACT OF THE DISCLOSURE

In the design of integrated circuits, a computer controlled method for the rough placement of cells. Initially, a synthesis tool is used to generate a netlist according to HDL, user constraint, and technology data. Thereupon, a cell separation process assigns (x,y) locations to each of the cells. The cell location information is supplied to the synthesis tool, which can then make changes to the netlist thereto. In the present invention, the size of the placement area is allowed to be scaled according to the new netlist. Next, the cells are spaced apart according to a spacing algorithm. A partitioning algorithm is then applied to group the cells into a plurality of partitions. A number of iterations of cell separation, synthesis of new netlist, size adjustment (if necessary), spacing, and partitioning are performed until the cells converge. Thereupon, detailed placement and routing processes are used to complete the layout.